IN THE CLAIMS

1. (Original) A double data rate memory device, comprising:

a first memory array;

a second memory array;

a mux control adapted to receive control signals;

a first pipeline coupled to the first memory array and the second memory array, wherein the first pipeline passes data from one of the first memory array and the second memory array and through the first pipeline on a rising edge of an external clock;

a second pipeline coupled to the first memory array and the second memory array, wherein the second pipeline passes data from the first memory array and the second memory array and through the second pipeline on a falling edge of the external clock;

wherein the first pipeline further comprises a first data mux connected to the mux control, the first memory array and the second memory array, the first data mux being adapted to direct data from one of the first memory array and the second memory array to the first pipeline; and

wherein the second pipeline further comprises a second data mux connected to the mux control, the first memory array and the second memory array, the second data mux being adapted to direct data from one of the first memory array and the second memory array to the second pipeline.

2. (Original) The memory device of claim 1, wherein mux control is adapted to receive address signals and clock signals.

3. (Original) The memory device of claim 1, wherein the first pipeline includes a plurality of latches.

4. (Original) The memory device of claim 3, wherein the second pipeline includes a further plurality of latches.

5. (Original) The memory device of claim 1, wherein the mux control determines which of the first pipeline and the second pipeline data from the first and second arrays is placed on.

6. (Original) The memory device of claim 1, wherein the first pipeline further comprises a first delay lock loop latch.

7. (Original) The memory device of claim 6, wherein the second pipeline further comprises a second delay lock loop latch.

8. (Original) The memory device of claim 7, wherein the at least one of the first latch and the second latch is operated by the mux control.

9. (Original) A double data rate memory device, comprising:

a first memory array;

a second memory array;

a control unit;

a first pipeline coupled to the control unit, the first memory array and the second memory array, wherein the first pipeline passes data from one of the first memory array and the second memory array and through the first pipeline on a rising edge of an external clock;

a second pipeline coupled to the control unit, the first memory array and the second memory array, wherein the second pipeline passes data from the first memory array and the second memory array and through the second pipeline on a falling edge of the external clock; and

wherein the control unit signals the first and second pipelines to pass data based on latency and clock cycle time.

10. (Original) The memory device of claim 9, wherein the first pipeline and the second pipeline include a first plurality of latches and a second plurality of latches, respectively.

11. (Original) The memory device of claim 9, wherein the first pipeline further comprises a first delay lock loop latch.

12. (Original) The memory device of claim 11, wherein the second pipeline further comprises a second delay lock loop latch.

13. (Original) The memory device of claim 12, wherein the at least one of the first latch and the second latch is operated by the mux control.

14. (Previously Presented) A double data rate memory device, comprising:

a first memory array;

a second memory array;

a first pipeline coupled to the first memory array and the second memory array, wherein the first pipeline passes data from one of the first memory array and the second memory array and through the first pipeline on a rising edge of an external clock;

a second pipeline coupled to the first memory array and the second memory array, wherein the second pipeline passes data from one of the first memory array and the second memory array and through the second pipeline on a falling edge of the external clock;

a control unit connected to the first and second pipelines; and

wherein the control unit generates an internal clock.

15. (Original) The memory device of claim 14, wherein the first pipeline includes a first plurality of stages, the second pipeline includes a second plurality of stages, and wherein the control unit controls the passing of data among the stages of the first and second pipelines.

16. (Original) An integrated circuit, comprising:

a first array of memory cells having first data;

a second array of memory cells having second data;

a first pipeline operable for outputting data on a rising edge of a clock, the first pipeline having a first data mux connected to the first array and a first latch;

a second pipeline, in parallel with the first pipeline, operable for outputting data on a falling edge of the clock, the second pipeline having a second data mux connected to the second array and a second latch;

a data mux controller connected to the first and second data muxes to direct the first data to the first pipeline and to direct the second data to the second pipeline; and

wherein the first data mux is further connected to the second array.

17. (Original) The integrated circuit of claim 16, further comprising a control unit connected to the first pipeline and the second pipeline, wherein the control unit synchronizes the output of data with the clock by utilizing propagation time of the pipelines.

18. (Original) The integrated circuit of claim 16, wherein the first and second arrays are physically located in a memory array.

19. (Original) The integrated circuit of claim 16, wherein the first array is physically located separately from the second array.

20. (Original) The integrated circuit of claim 16, wherein the first pipeline further comprises at least two latches connected in series.

21. (Original) The integrated circuit of claim 20, wherein the second pipeline further comprises at least two latches connected in series.

22. (Original) The integrated circuit of claim 21, wherein the second data mux is further connected to the first array.

23. (Original) An integrated circuit, comprising:

a first array of memory cells having first data;

a second array of memory cells having second data;

a first pipeline operable for outputting data on a rising edge of a clock, the first pipeline having a first data mux connected to the first array and a first latch;

a second pipeline, in parallel with the first pipeline, operable for outputting data on a falling edge of the clock, the second pipeline having a second data mux connected to the second array and a second latch;

a data mux controller connected to the first and second data muxes to direct the first data to the first pipeline and to direct the second data to the second pipeline;

wherein the first data mux is further connected to the second array; and

an output buffer connected to the first and second pipeline.

24. (Original) The integrated circuit of claim 23, wherein the first pipeline further comprises at least two latches connected in series.

25. (Original) The integrated circuit of claim 24, wherein the second pipeline further comprises at least two further latches connected in series.

26. (Original) The integrated circuit of claim 23, wherein the output buffer is adapted to receive data on the rising edge of a clock and the falling edge of a clock.

27. (Original) The integrated circuit of claim 26, wherein the output buffer is adapted to output data to at least one of a processor and a disk drive.

28. (Original) The integrated circuit of claim 23, wherein the first pipeline further comprises a first delay lock loop latch, and wherein the second pipeline further comprises a second delay lock loop latch.

29. (Original) The integrated circuit of claim 28, wherein the at least one of the first latch and the second latch is operated by the data mux controller.

30. (Original) The integrated circuit of claim 23, wherein a rising edge latch operates on a rising edge of an internal clock and a falling edge latch operates on a falling edge of the internal clock, the internal clock operates in advance of the clock.

31. (Original) An integrated circuit comprising:

a first memory array;

a second memory array;

a first pipeline, having a first data mux connected to the first memory array and the second memory array, for outputting data on a rising edge of a clock;

a second pipeline, having a second data mux connected to the first memory array and the second memory array, for outputting data on a falling edge of the clock; and

a data mux controller connected to the first and second data muxes to direct data from the first memory array and the second memory array to the first pipeline and the second pipeline.

32. (Original) An integrated circuit comprising:

a first memory array;

a second memory array;

a first pipeline having a first data mux connected to the first memory array and the second memory array, at least one first latch connected in series to the first data mux, and a first delay lock loop latch connected to the first latch;

a second pipeline having a second data mux connected to the first memory array and the second memory array, at least one second latch connected in series to the second data mux and a second delay lock loop latch connected to the second latch;

a data mux controller connected to the first and second data muxes to direct first data to the first pipeline and second data to the second pipeline; and

a control unit, having an internal clock, connected to the first and second pipelines, to synchronize output of data with rising and falling edges of an external clock.

33. (Original) The integrated circuit of claim 32, wherein the data mux controller is adapted to simultaneously direct first data to the first pipeline and second data to the second pipeline.

34. (Original) The integrated circuit of claim 32, wherein the control unit signals the first delay lock loop latch to pass first data to an output buffer and signals the second delay lock loop latch to pass second data to an output buffer.

35. (Original) The integrated circuit of claim 32, wherein the control unit, having an internal clock, connected to the first and second pipelines, to synchronize output of data with rising and falling edges of an external clock.

36-43. (Canceled)

44. (Currently Amended) A method for reading data on a memory device having a storage unit, a first pipeline, a second pipeline, and an output buffer, comprising:

selecting data in a storage unit to be placed on either of the first pipeline or the second pipeline;

determining which of the first or second pipeline data is to be placed on;

passing the data to the determined pipeline; and

passing data from the pipeline to the output buffer.

45. (Previously Presented) The method according to claim 44, wherein determining includes selecting a pipeline that can output data on rising edges of an external clock.

46. (Previously Presented) The method according to claim 44, wherein determining includes selecting a pipeline that can output data on falling edges of an external clock.

47. (Previously Presented) The method according to claim 45, wherein the determining includes determining based on the address of the data.

48. (Previously Presented) The method according to claim 45, wherein the determining includes determining based on latency of data.

49. (Previously Presented) The method according to claim 45, wherein the determining includes determining based on a combination of the address of the data and the latency of the data.

50. (Previously Presented) The method according to claim 46 wherein determining includes determining based on the address of the data.

51. (Previously Presented) The method according to claim 46, wherein determining includes determining based on latency of data.

52. (Previously Presented) The method according to claim 46, wherein said determination is based on a combination of the address of the data and the latency of the data.

53. (Currently Amended) A method for reading data on a memory device having a storage unit, a first pipeline, a second pipeline, and an output buffer comprising:

first determining which of the first or second pipeline a first piece of data is to be placed on;

first passing a first piece of data from the storage unit through a multiplexer to the first determined pipeline;

second determining which of the first or second pipeline a second piece of data is to be placed on;

second passing a second piece of data from the storage unit through a multiplexer to the second determined pipeline;

further determining which of the first or second pipeline further pieces of data are to be placed on;

further passing pieces of data from the storage unit through a multiplexer to the further determined pipeline; and

passing data to the output buffer from the pipeline.

54. (Previously Presented) The method of claim 53, wherein the first passing and the second passing occur simultaneously.

55. (Previously Presented) The method of claim 53, wherein the first passing and the second passing occur alternatingly.

56. (Previously Presented) The method of claim 53, wherein further passing occurs simultaneously with additional passing of pieces of data.

57. (Previously Presented) The method of claim 53, wherein further passing occurs alternatingly with additional passing of pieces of data.

58. (Currently Amended) A method for reading data comprising:

selecting data in a storage unit that is connected to both a first pipeline and a second pipeline such that data in the storage unit can be placed onto either of the first pipeline or the second pipeline;

determining which of a first pipeline and a second pipeline the data is to be placed on;

passing the data to the determined pipeline;

passing data from the pipeline to an output buffer; and

timing the passing.

59. (Previously Presented) The method of claim 58, wherein the timing is such that data passed from the pipelines to the output buffer can be read on rising and falling edges of an external clock.

60. (Previously Presented) The method of claim 58, wherein the timing is adjusted based on cycle time.

61. (Previously Presented) The method of claim 58, wherein the timing is adjusted based on latency.

62. (Previously Presented) The method of claim 58, wherein the timing is adjusted based on some combination of cycle time and latency.

63. (Previously Presented) The method of claim 58, wherein the timing is set such that data can be read on a first and second event.

64. (Currently Amended) A method of reading data comprising:

issuing a read command;

selecting from a plurality of pipelines;

first passing a first piece of data from a memory location through a multiplexer to the first selected pipeline; ~~and~~

second passing ~~a~~ the first piece of data from the first selected pipeline to a system device;

passing a second piece of data from a subsequent memory location through a multiplexer to a further selected pipeline; and

passing the second piece of data from the further selected pipeline to the system device.

65. (Previously Presented) The method of claim 64, wherein the read command is a processor request to read the data of a certain memory location.

66. (Previously Presented) The method of claim 65, wherein the certain memory location is a storage unit.

67. (Previously Presented) The method of claim 65, wherein the certain memory location is an array.

68. (Previously Presented) The method of claim 65, wherein the certain memory location is a memory device.

69. (Previously Presented) The method of claim 64, wherein the system device is a processor.

70. (Previously Presented) The method of claim 64, wherein the system device is a memory device.

71. – 76. (Canceled)